WHAT IS CLAIMED IS:

1. A switch comprising:

A plurality of ports for exchanging data, and a shared-memory for enabling the exchange of data between first and second ones of said ports, said shared-memory comprising:

An array of memory cells arranged as a plurality of rows and a single column having a width equal to a predetermined word-width;

Circuitry for writing selected data presented at said first one of said ports to a selected row in said array as a word of the predetermined word-width during a first time period and for reading said selected data as a word of the predetermined word-width from said selected row during a second time period for output at said second one of said ports.

2. The switch of Claim 1 and further comprising a buffer associated with each port for converting words of data from an initial bit-width to said predetermined bit width.

3. The switch of Claim 1 wherein said predetermined bit-width is equal to a bit-width of certain bit width and associated overhead.

4. The switch of Claim 2 wherein said initial bit-width is 48 bits and said predetermined bit-width is 384 bits.

5. The switch of Claim 1 wherein said circuitry for reading and writing comprises an available address table for storing write addresses available for selection and use in writing to selected rows said array.

6. The switch of Claim 5 wherein said circuitry for reading and writing further comprises a used address table for storing addresses already used for writing data to selected rows in said array.

7. The switch of Claim 1 wherein said array comprises an array of random access memory cells of the read/write classification.

8. A shared-memory switch comprising:

A plurality of ports for exchanging data between external devices associated with each of said ports;

A buffer associated with each of said ports for assembling a stream of data words being input into said switch into a single word of a predetermined width and for converting single data words of said predetermined width being output from said switch into a stream of data words;

A shared-memory for effectuating a transfer of data from a first one of said ports to a second one of said ports through corresponding ones of said buffers, said shared-memory comprising a plurality of banks each having an array of memory cells arranged as a plurality of rows and a single column of said predetermined width and circuitry for selecting a said row in response to a received address;

A plurality of available address tables each for maintaining a queue of addresses available for writing said single words of data to a corresponding one of said banks; and

A plurality of used address tables each for maintaining a queue of addresses for reading from a corresponding one of said banks.

9. The switch of Claim 8 wherein said streams of data words comprise eight forty-eight bit words of ATM data and said single words have a said predetermined width of 384 bits.

10. The switch of Claim 8 wherein each of said plurality of available address tables comprises a first-in-first-out memory.

11. The switch of Claim 8 wherein each of said plurality of used address tables comprises a random access memory, that performs read and write operations.

12. The switch of Claim 8 wherein each of said banks is randomly accessible.

13. The switch of Claim 8 wherein each of said banks stores data corresponding to a selected said port from which data is to be read.

14. The switch of Claim 8 wherein each of said banks stores data corresponding to a plurality of ports from which data is to be read in a selected order.

15. The switch of Claim 8 wherein said shared-memory comprises i number of banks and said switch comprises j number of ports, where $i < j$.

16. A digital information system comprising:

First and second resources operable to exchange data in a selected digital format; and

A digital switch comprising:

First and second ports for selectively coupling said first and second resources; and

A shared memory for enabling the exchange of data between said first and second ports as words of a predetermined word-width, said shared-memory comprising:

An array of memory cells arranged as a plurality of rows and a single column having a width equal to said predetermined word-width; and

Circuitry for writing a selected data word presented at said first one of said ports to a selected row in said array during a first time period and for reading said selected data word from said selected row during a second time period to said second one of said ports.

17. The system of Claim 16 wherein data are exchanged through said ports as streams of data words of an initial word-width and said switch further comprises buffers for converting data words between said initial word-width and said predetermined word-width.

18. The system of Claim 16 wherein said selected digital format comprises as Asynchronous Transfer Mode digital data format.

19. The system of Claim 18 wherein said predetermined word-width equals a bit-width of a user data portion of an asynchronous transfer mode information packet.

20. The system of Claim 16 wherein said first and second resources are selected from the group comprising digital telephones, digital facsimile machines, digital data networks, home networks, digital private branch exchanges, workstations and video teleconferencing equipment.

21. The system of Claim 16 where the data interface is selected from the group consisting of DDR (double data rate), QDR (quad data rate), Rambus™, and programmable bit burst length interfaces.

22. A method of switching a plurality streams of data each comprising a selected number of words, the method comprising the steps of:

Receiving a first one of the streams of data at a first port to a shared-memory switch during a first write period;

Storing the first stream of data as a first single data word in a first row in shared-memory within the shared-memory switch from which the first single data word is to be subsequently retrieved;

Receiving a second one of the streams of data at a second port to the shared-memory switch during a second write period;

Storing the second stream of data as a second single data word in a second row in shared-memory within the shared-memory switch from which the second data word is to be subsequently retrieved;

Retrieving the first single data word from the first row in shared-memory during a first read period and outputting the first single word of data as the first stream of data through a selected port of the switch; and

Retrieving the second data word from the second row in shared-memory during a second read period and outputting the second single word of data as the second stream of data through a selected port of the switch.

23. The method of Claim 22 and further comprising the step of selecting the first and second rows from a single cell array in shared-memory.

24. The method of Claim 22 and further comprising the step of selecting the first and second rows from respective first and second cell arrays in shared-memory.

25. The method of Claim 22 and further comprising the step of spacing the second write period and the first read period by a selected number of intervening time periods.

26. The method of Claim 25 and further comprising the step of refreshing selected rows in shared-memory during the selected number of intervening time periods.

27. The method of Claim 22 wherein said steps of storing comprise the substeps of addressing the shared-memory to access the first and second rows by retrieving addresses from at least one available address table associated with the shared memory.

28. The method of above claims where ATM protocol is only exemplary, and the claims are applicable to other protocols which comprise fixed or variable bit widths and overhead, whether they are pre-determined or programmable.

29. A switch compromising:

A plurality of ports for exchanging data, and a shared memory enabling the exchange of data between first and second one of said ports, said shared memory comprising:

An array of memory cells arranged as a plurality of rows and columns having a programmable word-width circuitry for writing selected data presented at said first one of said ports to a selected row and column set in said array as a word of the programmable word-width during a first time period and for reading said select as a word of the programmable word-width from a select row and column set during a second time period for output at said second one of said ports.

30. The method of claim 22 where address, command, control and data are strobed on both the raising and falling edges of system clock.

31. An electronic system comprising:

At least one logic processor, memory, and input/output circuitry, with the memory consisting of an array of memory cells arranged as a plurality of banks, rows and columns having a programmable word width.

32. A single chip electronic system comprising:

At least one logic processor, memory, and input output circuitry, with the memory consisting of an array of memory cells arranged as a plurality of banks, rows and columns having a programmable word width.